What is claimed is:

Claim 1. In an emulation engine comprised of a plurality of modules, a work station, and a maintenance bus for transferring data between the work station and said modules, each of said modules including a plurality of module processors and a module main memory unit accessible for data transfers during an emulation by each of said plurality of processors, each of said processors having a control store to store a programmable sequence of emulation steps that define logic states for its processor, a method to allow data transfers between said module main memory unit and said work station without interrupting an in progress emulation, including the steps of:

  compiling said programmable sequence of emulation steps to include, in at least one step, a blocking code that is decoded, when the step is read from the control store, as a disable command between the plurality of module processors and said module main memory;

  decoding said blocking code and, in response thereto, blocking transfers between the plurality of module processors and said module main memory; and

  transferring data between said work station and said module main memory while transfers between the plurality of module processors and said module main memory are blocked.

Claim 2. A method to allow data transfers between said module main memory unit and said work station as in claim 1 further including the step of unblocking transfers between the plurality of module processors and said module main memory when the step is decoded that is next in the sequence after said step that includes said blocking code.

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Claim 3. A method to allow data transfers between said
module main memory unit and said work station as in claim 1
3   wherein said programmable sequence is repeated and said
4   decoding and transferring steps are repeated with each
5   repetition of said programmable sequence.

1   Claim 4. A method to allow data transfers between said
2   module main memory unit and said work station as in claim 2
3   wherein said programmable sequence is repeated and said
4   decoding and transferring steps are repeated with each
5   repetition of said programmable sequence.

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